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COMPUTER SCIENCE & IT

OBJECTIVE PRACTICE SETS VOLUME - II

CONTENTS

DIGITAL LOGIC

OBJECTIVE PRACTICE SETS

Page No. 1 - 75

1 CHAPTER

Basics of Digital Logic

Multiple Choice Questions & NAT Questions

Q.1 $(10110011100011110000)_2$ in base 32 is
(a) 2214716 (b) 1192331
(c) 11976 (d) 11142316

Q.2 The hexadecimal representation of $(657)_8$ is
(a) $(1AF)_H$ (b) $(D78)_H$
(c) $(D71)_H$ (d) $(32F)_H$

Q.3 The binary equivalent of the decimal number 0.4375 is
(a) 0.0111 (b) 0.1011
(c) 0.1100 (d) 0.1010

Q.4 Zero has two representations in
(a) Sign magnitude (b) 1's complement
(c) 2's complement (d) Both (a) and (b)

Q.5 Which of the following code is a weighted code?
(a) Gray (b) Excess-3
(c) Shift counter (d) 5111

Q.6 In signal magnitude representation, the binary equivalent of 22.5625 is (the bit before comma represents the sign).
(a) 0, 10110.1011 (b) 0, 10110.1001
(c) 1, 10101.1001 (d) 1,10110.1001

Q.7 A variable takes thirteen possible values. It can be communicated using
(a) Thirteen bits (b) Three bits
(c) $\log_2^{13}$ bits (d) Four bits

Q.8 Convert $(-54)_{10}$ to hexadecimal.
(a) $(34)_{16}$ (b) $(CA)_{16}$
(c) $(54)_{16}$ (d) $(DA)_{16}$

Q.9 The 2's complement representation of $(539)_{10}$ in hexadecimal is
(a) ABE (b) DBC
(c) DE5 (d) 21B

Q.10 What is 2's complement of $(101)_3$?
(a) $(010)_3$ (b) $(011)_3$
(c) $(121)_3$ (d) $(121)_2$

Q.11 Which of the following decimal numbers can be exactly represented in binary notation with a finite number of bits?
(a) 0.1 (b) 0.2
(c) 0.4 (d) 0.5

Q.12 A particular number system has 18 symbols from 0 to 9, A, B, C, E, S, G, T. If two numbers GATE and CSE are given to an adder, then output of adder is
(a) TC7A (b) T5EA
(c) G5SA (d) T5SA

Q.13 The square of octal number 23 is
(a) 529 (b) 539
(c) 551 (d) 650

Q.14 If $(123)_5 = (X3)_Y$, then the number of possible values of x is
(a) 4 (b) 3
(c) 2 (d) 1

Q.15 If $(2.3)_{\text{base 4}} + (1.2)_{\text{base 4}} = (y)_{\text{base 4}}$, what is the value of y?
(a) 10.1 (b) 10.01
(c) 10.2 (d) 1.02

Q.16 F's complement of $(2BFD)_{16}$ is
(a) E304 (b) D403
(c) D402 (d) C403

Q.17 Which of the following weighted code will give 9's complement by complementing each individual bit?
(a) Excess-3 (b) 5421
(c) 2421 (d) Both (a) and (c)

Q.18 Consider a system which has two eight bit inputs D_1 = 01010101, D_2 = 00000000, the system produces eight bit output that is bitwise XOR of the inputs. The eight bit output of system is input to the Gray Code Converter. The decimal equivalent of the output from Gray Code converter is _____.

Q.19 Which of the following statement is Incorrect for the range of n bit binary numbers?
(a) Range of unsigned numbers is 0 to $2^n - 1$.
(b) Range of signed number is $-2^{n-1} + 1$ to $2^{n-1} - 1$.
(c) Range of signed 1's complement numbers is $-2^{n-1} + 1$ to 2^{n-1}.
(d) Range of signed 2's complement numbers is -2^{n-1} to $2^{n-1} - 1$.

Q.20 The greatest negative number which can be stored in computer that has 8-bit word length and uses 2's complement arithmetic is
(a) –256 (b) –255
(c) –128 (d) –127

Q.21 Correct $(1101)_2$ is corresponding excess-3.
(a) 00010000 (b) 01000110
(c) 00100110 (d) 00010110

Q.22 Find the value of x in the given equation
$$(2)_3 + (3)_4 = (x)_5$$

Q.23 What are the value of R_1 and R_2 respectively in the expression $(235)_{R1} = (565)_{10} = (1065)_{R2}$
(a) 8, 16 (b) 16, 8
(c) 6, 16 (d) 12, 8

Q.24 Convert $(3121.121)_4$ to base 3?
(a) 10022.100 (b) 22001.100
(c) 22001.101 (d) 10022.110

Q.25 The number of 1's in the binary representation of (3 * 4096 + 15 * 256 + 5 * 16 + 3) are
(a) 8 (b) 9
(c) 10 (d) 12

Q.26 Two numbers –48 and –23 are added using 2's complement. The 2's complement of the result using 8 bit representation is _____.
(a) 10111001 (b) 01000111
(c) 01101010 (d) 11100111

Q.27 A number in 4-bit two's complement representation is $X_3\ X_2\ X_1\ X_0$. This number when stored using 8 bits will be
(a) $0\ 0\ 0\ 0\ X_3\ X_2\ X_1\ X_0$
(b) $1\ 1\ 1\ 1\ X_3\ X_2\ X_1\ X_0$
(c) $X_3\ X_3\ X_3\ X_3\ X_3\ X_2\ X_1\ X_0$
(d) $\bar{X}_3\bar{X}_3\bar{X}_3\bar{X}_3\bar{X}_3X_2X_1X_0$

Q.28 Result of the subtraction with the following unsigned decimal numbers by taking the 10's complement of the subtrahend. 1753 – 8640
(a) 3113 (b) 10393
(c) –6887 (d) –3113

Q.29 Given that $(EOB)_H - (ABF)_H = Y$. The radix 8's complement of Y is
(a) 844 (b) 1514
(c) 6264 (d) 3251

Q.30 Let A = 1111 1010 and B = 0000 1010 be two 8 bit 2's complement numbers. Their product in 2's complement is
(a) 1100 0100 (b) 1001 1100
(c) 1010 0101 (d) 1101 0101

Q.31 If $(11x1y)_8 = (12C9)_{16}$ then the values of x and y are
(a) 3 and 1 (b) 5 and 7
(c) 7 and 5 (d) 1 and 5

Q.32 $(FE35)_{16}$ XOR $(CB15)_6$ is equal to
(a) $(3320)_{16}$
(b) $(FF35)_{16}$
(c) $(FF50)_{16}$
(d) $(3520)_{16}$

Q.33 Which of the following represents $(E3)_{16}$?
(a) $(1CE)_{16} + (A2)_{16}$
(b) $(1BC)_{16} - (DE)_{16}$
(c) $(2BC)_{16} - (1DE)_{16}$
(d) $(200)_{16} - (11D)_{16}$

Q.34 $(X)_8$ is expressed in Gray code as $(11110)_2$. The value of X is _____.

Q.35 Given $(135)_{\text{base } x} + (144)_{\text{base } x} = (323)_{\text{base } x}$. The value of base x is _____.

Q.36 The minimum decimal equivalent of the number 11C.0 is _____.

Q.37 The number of 1's in 8-bits representation of –127 in 2's complement form is m and that in 1's complement form is n. What is the value of m/n?

Q.38 If $(28)_x$ in base x number system is equal to $(37)_y$ in base y number system, the possible values of x and y are:
(a) 5, 3 (b) 8, 7
(c) 3, 4 (d) 13, 9

Answers Basics of Digital Logic

1.	(a)	2.	(a)	3.	(a)	4.	(d)	5.	(d)	6.	(b)	7.	(d)	8.	(b)	9.	(d)
10.	(c)	11.	(d)	12.	(d)	13.	(c)	14.	(c)	15.	(a)	16.	(c)	17.	(c)	18.	(127)
19.	(c)	20.	(c)	21.	(b)	22.	(10)	23.	(b)	24.	(c)	25.	(c)	26.	(b)	27.	(c)
28.	(c)	29.	(c)	30.	(a)	31.	(a)	32.	(d)	33.	(d)	34.	(24)	35.	(6)	36.	(194)
37.	(2)	38.	(d)	39.	(c)	40.	(a)	41.	(a)	42.	(33)	43.	(d)	44.	(a)	45.	(a)
46.	(d)	47.	(1101)	48.	(c)	49.	(c)	50.	(15)	51.	(54)	52.	(d)	53.	(a, c)	54.	(b, d)
55.	(c, d)	56.	(b, c)	57.	(b, c)	58.	(a, b)	59.	(b, c)	60.	(a, b, c)						

Explanations Basics of Digital Logic

1. (a)

To convert to base 8, we group in 3's because $2^3 = 8$.

To convert to base 16, we group in 4's because $2^4 = 16$.

To convert to base 32, we group in 5's because $2^5 = 32$.

Grouping in 5's, from the right we get the answer.

So $\underset{22}{\underline{10110}}$ $\underset{14}{\underline{01110}}$ $\underset{7}{\underline{00111}}$ $\underset{16}{\underline{10000}}$

2. (a)

Octal number 657_8

Binary representation of 657_8

$$\underline{0\,0\,0\,1}\ \underline{1\,0\,1\,0}\ \underline{1\,1\,1\,1}$$

Hexadecimal representation of $(657)_8$

$= (1\,AF)_H$

3. (a)

$(0.4375)_{10}$

(i) $0.4375 \times 2 = 0.8750$ → 0

(ii) $0.8750 \times 2 = 1.7500$ → 1

(iii) $0.75 \times 2 = 1.50$ → 1

(iv) $0.50 \times 2 = 1.0$ → 1

$\therefore (0.4375)_{10} = (0.0111)_2$

Hence, (a) is correct option

4. (d)

Zero has two representations in sign magnitude:

1. MSB is 0.
2. MSB is 1.

Both of these representations have equal value i.e., 0.

In 1's complement, 0 has two representations.

1. All bits are zero. 2. All bits are 1.

5. (d)

Weighted codes are the ones in which every bit position is assigned a weight.

$\therefore$ 5111 is a weighted code where the weight for MSB is 5 and for LSB is 1.

6. (b)

Sign bit must be 0 (+ve number)

$(22)_{10} = (10110)_2$

$(0.5625)_{10} = (0.1001)_2$

$0.5625 \times 2 = 1.125$

$0.125 \times 2 = 0.25$

$0.25 \times 2 = 0.5$

$0.5 \times 2 = 1.0$

$\therefore$ Correct answer is 0, 10110.1001.

7. (d)

As there are only 13 possible values, a variable can take, we need to use $\lceil \log_2^{13} \rceil$ bits = 4 bits.

8. (b)

$(54)_{10}$ in 8 bit binary is $(00110110)_2$

$(-54)_{10}$ in 2's complement representation is $(11001010)_2$.

Now, grouping 4 digits each from LSB to MSB, we get $(CA)_{16}$.

9. (d)

$(539)_{10}$ in 2's complement representation is $(0010\ 0001\ 1011)_2$ which is equivalent to $(21B)_{16}$.

10. (c)

2's complement of $(101)_3 = 222 - 101 = (121)_3$

[$\because$ $(r-1)$'s complement]

11. (d)

0.5 is the only decimal number which has a terminating binary representation.

$$(0.5)_{10} = (0.1)_2$$
$$(0.1)_{10} = (0.00011....)_2$$
$$(0.2)_{10} = (0.00110....)_2$$
$$(0.4)_{10} = (0.01100....)_2$$

12. (d)

GATE + CSE

This is Base 18 number system

$$E + E = 14 + 14 = 28 = (1A)_{18}$$
$$T + S + \text{carry} = 17 + 15 + 1 = 33 = (1S)_{18}$$
$$A + C + \text{carry} = 10 + 12 + 1 - 23 = (15)_{18}$$
$$G + \text{carry} = 16 + 1 = (17) = T$$

$\therefore$ Answer is T5SA

13. (c)

$$(23)_8 = (19)_{10}$$
$$\text{Square of } (19)_{10} = (361)_{10}$$
$$\therefore \quad (361)_{10} = (551)_8$$

14. (c)

$$(123)_5 = (X3)_Y$$

As we can observe that

$$5^2 \times 1 + 2 \times 5^1 + 3 \times 5^0 = Y' \times X + 3XY^{\circ}$$

$$25 + 10 + \cancel{3} = YX + \cancel{3}$$
$$35 = YX$$

Since Y is the base, $Y > X$ and $Y > 3$

$\therefore$ Possible values are given by

$$X = \frac{35}{Y}$$

When $Y = 7$, $X = 5$ and $Y = 35$, $X = 1$

Hence (c) is the correct option.

Note that ($X = 7$, $Y = 5$) and ($X = 35$, $Y = 1$) are not possible.

15. (a)

$$\begin{array}{r} 1 \\ 2.3 \\ +1.2 \\ \hline 10.1 \end{array}$$

$$3 + 2 = (5)_{10} = (11)_4$$

16. (c)

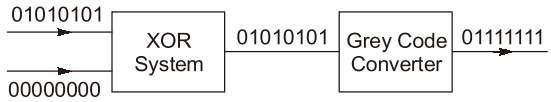
$(2BFD)_{16}$

$$\begin{array}{r} FFFF \\ -2BFD \\ \hline D402 \end{array}$$

17. (c)

Both Excess 3 codes and 2421 codes have this property and therefore, are called self complementary codes. But since the question requires weighted codes, the answer is '2421'.

18. (127)



Decimal equivalent of 01111111 = 127.

19. (c)

Range of signed 1's complement numbers is $-2^{n-1} + 1$ to $2^{n-1} - 1$.

20. (c)

Range of integers that can be represented by a n bit two's complement representation is -2^{n-1} to $(2^{n-1} - 1)$.

Here, $n = 8$

$\therefore$ The greatest negative number which can be stored $= -2^7 = -128$.

21. (b)

Excess-3 is obtained when 3 is added to every digit of the BCD code.

$(1101)_2 = (13)_{10}$

$(13)_{10}$ in BCD is

To convert to excess 3.

$$\begin{array}{r} 0001\ 0011 \\ +0011\ 0011 \\ \hline 0100\ 0110 \end{array}$$

22. (10)

$$(2)_3 = (2)_{10}$$
$$(3)_4 = (3)_{10}$$
$$(2)_{10} + (3)_{10} = (5)_{10} = (10)_5$$
$$\therefore \quad x = 10$$

23. (b)

$$(235)_{R_1} = \left(2R_1^2 + 3R_1 + 5\right)_{10} = (565)_{10}$$

Using the options, we can find out that R_1 must be 16.

$$(1065)_{R2} = ((R_2)^3 + 6R_2 + 5)_{10} = (565)_{10}$$

$R_2 = 8$ satisfies this equation.

Note: $(235)_{R_1} = (565)_{10} = (1065)_{R_2}$

COMPUTER ORGANIZATION & ARCHITECTURE

OBJECTIVE PRACTICE SETS

Page No. 76 - 162

1 CHAPTER
Basics of Computer Design

Multiple Choice Questions & NAT Questions

Q.1 The computer performs all mathematical and logical operations inside its
(a) Memory unit (b) Central processing unit
(c) Output unit (d) Visual display unit

Q.2 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Pointer
B. Position Independent code
C. Constant operand

List-II
1. Indirect AM
2. Immediate AM
3. Relative AM

Code:

	A	B	C
(a)	1	2	3
(b)	3	2	1
(c)	1	3	2
(d)	2	3	1

Q.3 The most appropriate matching of the following pairs is

Column 1	Column 2
X: Indirect addressing	1. Loops
Y: Immediate addressing	2. Pointers
Z: Auto-decrement address	3. Constant

(a) X-2, Y-3, Z-1 (b) X-3, Y-2, Z-1
(c) X-1, Y-3, Z-2 (d) X-3, Y-1, Z-2

Q.4 Consider the following I/O instruction format for IBM 370 I/O channel

Operation Code	Channel Address	Device Address

Then operation code specifies
1. Test I/O
2. Test channel
3. Store channel identification
4. Halt device

(a) Only 1 and 4 (b) Only 2 and 3
(c) 1, 2, 3 and 4 (d) Only 1, 3 and 4

Q.5 An interrupt that can be temporarily ignored by the counter is known as
(a) Vectored interrupt
(b) Non-maskable interrupt
(c) Maskable interrupt
(d) Low priority interrupt

Q.6 A processor can support a maximum memory of 4 GB where memory is word addressable and word is 2 bytes. What will be the size of the address bus of the processor?
(a) At least 2 bytes (b) At least 28 bits
(c) At least 31 bits (d) Minimum 4 bytes

Q.7 A digital computer has memory unit with 24 bits word. The instruction set consists of 150 different operations. All instructions have an operation code part and an address part. Each instruction is stored in one word of memory. How many bits are needed for the OPCODE and how many bits are left for the address of the instruction.
(a) 8, 16 (b) 16, 64
(c) 4, 8 (d) 8, 64

Q.8 An instruction is stored at location 300 with its address field. At location 301 the address field has value 400. A processor register R1 contains the number 200. Evaluate the effective address matching the following addressing modes to their respective addresses.

A. Direct	1. 702
B. Immediate	2. 200
C. Relative	3. 400
D. Register indirect	4. 600
E. Index (R1 is index)	5. 301

(a) A3 B5 D2 E4 C1 (b) A3 B4 C1 D1 E5
(c) A5 B3 C2 D1 E4 (d) A4 B3 C1 D5 E2

Q.9 What is the most appropriate match for the items in the first column with the items in the second column:

Column 1:

X. Indirect addressing
Y. Indexed addressing
Z. Base register addressing

Column 2:

1. Array implementation
2. Writing relocatable code
3. Passing array as parameter

(a) X-3, Y-1, Z-2 (b) X-2, Y-3, Z-1
(c) X-3, Y-2, Z-1 (d) X-1, Y-3, Z-2

Q.10 In which of the following address mode, the content of the program counter is added to the address part of the instruction to get the effective address?

(a) Indexed addressing mode
(b) Implied addressing mode
(c) Relative addressing mode
(d) Register addressing mode

Q.11 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. Stack overflow
B. Supervisor call
C. Invalid opcode
D. Timer

List-II

1. Software interrupt
2. Internal interrupt
3. External interrupt
4. Machine check interrupt

Codes:

	A	B	C	D
(a)	2	3	4	1
(b)	2	1	2	3
(c)	3	1	2	4
(d)	3	1	4	2

Q.12 In a certain processor, a 2 byte Jump instruction is encountered at memory address 3010H, the Jump instruction is in PC relative mode. The instruction is JMP – 7 where – 7 is signed byte. Determine the Branch Target Address

(a) 300 BH (b) 3009 H
(c) 3003 H (d) 3007 H

Q.13 Processor *XYZ* supports only the immediate and the direct addressing modes. Which of the following programming language data structures cannot be implemented on this processors?

1. Pointers
2. Arrays
3. Records

(a) 1, 2 and 3 (b) 2 and 3
(c) 1 and 2 (d) Only 1

Q.14 Word 20 contains 40
Word 30 contains 50
Word 40 contains 60
Word 50 contains 70

Which of the following instructions loads 60 into the accumulator?

(a) Load immediate 20
(b) Load direct 30
(c) Load indirect 20
(d) Load indirect 30

Q.15 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I	**List-II**
A. $A[1] = B[J]$;	1. Indirect addressing
B. while [$*A$++];	2. Indexed addressing
C. int temp = $*x$;	3. Auto increment

Codes:

	A	B	C
(a)	3	2	1
(b)	1	3	2
(c)	2	3	1
(d)	1	2	3

Q.16 In immediate addressing mode, where is the operand placed?

(a) In memory
(b) In stack
(c) In CPU register
(d) In instruction after opcode

Q.17 If the last operand performed on a computer with an 8-bit word has an addition in which the two operands were 00000010 and 00000011, what would be value of the overflow, sign and half-carry flags respectively?

(a) 0, 1, 0 (b) 0, 1, 1
(c) 1, 0, 1 (d) 0, 0, 0

Q.18 A 4-byte long PC-relative branch instruction is fetched from memory address $(512)_{10}$ and while its execution, the branch is made to location $(885)_{10}$. What is unsigned displacement present in the instruction? (Relative value) _____?

Q.19 A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____.

Q.20 The register which contains the data to be written into or read out of the addressed location is known as
(a) Memory address register
(b) Memory data register
(c) Program computer
(d) Index register

Q.21 In four-address instruction format, the number of bytes required to encode an instruction is (assume each address requires 24 bits and 1 byte is required for operation code)
(a) 9 (b) 13
(c) 14 (d) 12

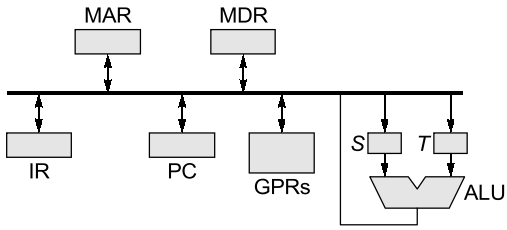
Q.22 The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the following program is executed.

MOVI Rs, 1;	Move immediate
LOAD Rd, 1000(Rs);	Load from memory
ADDI Rd, 1000;	Add immediate
STOREI 0(Rd), 20;	Store immediate

Which of the statements below is TRUE after the program is executed?
(a) memory location 1000 has value 20
(b) memory location 1020 has value 20
(c) memory location 1021 has value 20
(d) memory location 1001 has value 20

Q.23. A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?
(a) 400 (b) 500
(c) 600 (d) 700

Q.24 Consider the following data path of a CPU:



The, ALU the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycle are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory but into the MDR.

The instruction "add R_0, R_1" has the register transfer interpretation $R_0 <= R_0 + R_1$. The minimum number of clock cycles needed for execution cycle of this instruction is
(a) 2 (b) 3
(c) 4 (d) 5

Q.25 In the previous question the instruction "call *Rn*, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is
Rn < = PC + 1;
PC < = *M* [PC];
The minimum number of CPU clock cycles needed during the execution cycle of this instruction is
(a) 2 (b) 3
(c) 4 (d) 5

Q.26 Consider the following program segment:

	Instruction	Meaning	Size (words)
I_1	LOAD r_0, 500	r_0 – [500]	2
I_2	MOV r_1, r_0	$r_0 - r_0$	1
I_3	Add r_0, r_1	$r_0 - r_0 + r_1$	1
I_4	Inc r_0	$r_0 - r_0 + 1$	1
I_5	Inc r_1	$r_1 - r_1 + 1$	1
I_6	Add r_0, r_1	$r_0 - r_0 + r_1$	1
I_7	Store r_1, r_0	M[(r_1)r_0]	2
I_8	Halt	Stop	1

Assume that memory is word addressable with word size 32 bits. Program is loaded into memory location 3000 onwards. The value of PC at the end of execution of above program is _____.

Q.27 A computer has 32 bit instruction and 9-bit address. If there are 400 two address instructions then how many one address instructions can be formulated?

(a) 2^{14} (b) $2^{32} - 200$
(c) $2^{14} - 400$ (d) $(2^{14} - 400) \times 2^9$

Q.28 In which addressing mode, the effective address of the operand is generated by adding a constant value to the content of a register?

(a) Absolute mode (b) Indirect mode
(c) Immediate mode (d) Index mode

Q.29 A complier designer has to decide between two code sequences for a particular m/c. Here data shown below. So which of the code sequence is faster?

Instruction (log)	CPI
A	1
B	2
C	3

Code sequence	Instruction count		
	A	B	C
1	2	1	2
2	4	1	1

(a) Code sequence 1 is faster
(b) Code sequence 2 is faster
(c) Both are same
(d) None of these

Q.30 Consider a 16-bit processor in which the following one address Instruction appeals in main memory starting at location 200.

200	Opcode
201	500
202	Next Instruction
⋮	
500	999

There is also a base register that contains the value 100.

Match **List-I** (Mode) with **List-II** (Effective Address) and select the correct answer using the codes given below the lists:

	List-I		List-II
A.	Immediate	1.	600
B.	Direct	2.	999
C.	Memory Indirect	3.	201
D.	PC-relative	4.	500
E.	Base-register	5.	702

Codes:

	A	B	C	D	E
(a)	3	5	2	4	1
(b)	4	5	2	1	3
(c)	3	4	2	5	1
(d)	3	4	5	1	2

Q.31 The control word of micro programmed control is as follows:

condition	control field	next address

It has to generate 48 control signals, next addresses are selected based on 16 conditional or flag information. The control memory has 84 control programs of size 8 words.

What is the size (in bits) of control word in horizontal micro-programming? _____

Q.32 Most relevant addressing mode to write position independent code is

(a) direct (b) indirect
(c) relative (d) indexed mode

Q.33 Consider the following program segment. Here *R*1, *R*2 and *R*3 are the general purpose registers.

Instruction	Operation	Instruction Size (no. of words)
MOV *R*1, 3000	*R*1 ← *M*[3000]	2
Loop:		
MOV *R*2,(*R*1)	*R*2 ← *M*[*R*3]	1
ADD *R*2, *R*1	*R*2 ← *R*1 + *R*2	1
MOV (*R*3), *R*2	*M*(*R*3] ← *R*2	1
INC *R*3	*R*3 ← *R*3 + 1	1
DEC *R*1	*R*1 ← *R*1 – 1	1
BNZ LOOP	Branch on not zero	2
Halt	Stop	1

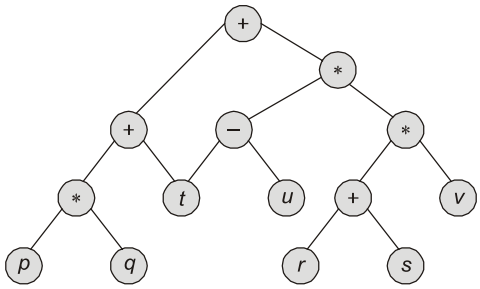
Assume that the content of memory location 3000 is 10 and the content of the register *R*3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 100. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

(a) 10 (b) 11
(c) 20 (d) 21

Q.34 Consider a processor with byte-addressable memory. Assume that all registers, including Program Counter (PC) and Program Status Word

in memory. The binary operators used in the tree can be evaluated by the machine only when all operands are in register. The instruction produce result only in a register.



What is the minimum number of registers needed to evaluate the expression if, no intermediate results can be stored in memory?

(a) 3 (b) 4
(c) 5 (d) 6

■■■■

Answers Basics of Computer Design

1.	(b)	2.	(c)	3.	(a)	4.	(c)	5.	(c)	6.	(c)	7.	(a)	8.	(a)	9.	(a)
10.	(c)	11.	(b)	12.	(a)	13.	(c)	14.	(c)	15.	(c)	16.	(d)	17.	(d)	18.	(369)
19.	(16383)	20.	(b)	21.	(b)	22.	(d)	23.	(c)	24.	(b)	25.	(b)	26.	(3009)	27.	(d)
28.	(d)	29.	(b)	30.	(c)	31.	(62)	32.	(c)	33.	(d)	34.	(d)	35.	(b)	36.	(c)
37.	(b)	38.	(c)	39.	(d)	40.	(b)	41.	(c)	42.	(b)	43.	(c)	44.	(d)	45.	(d)
46.	(c)	47.	(c)	48.	(a)	49.	(a)	50.	(c)	51.	(a)	52.	(c)	53.	(b)	54.	(a)
55.	(–128)	56.	(a)	57.	(a)	58.	(b)	59.	(d)	60.	(a)	61.	(d)	62.	(16)	63.	(d)
64.	(b)	65.	(c)	66.	(a)	67.	(d)	68.	(92)	69.	(2032)	70.	(c)	71.	(a)	72.	(b)
73.	(c)	74.	(b)	75.	(c)	76.	(2048)	77.	(d)	78.	(a, b, d)	79.	(c)	80.	(b, c)		
81.	(a, c)	82.	(b, c)	83.	(b)												

Explanations Basics of Computer Design

2. (c)

For making use of pointer in programs, indirect addressing mode is used.

Pointer stores the address of a variable and indirect addressing mode stores address of effective address the instruction.

Position independent code make use of relocation concept which is implemented by the use of relative addressing mode which uses relocation register to set the difference of logical and physical address.

Immediate addressing mode provides the value directly in the instruction which is suitable to be used for constant operands of the program.

4. (c)

The operation code specifies one of eight input output instructions: Start input/output, start input/output fast release, test input/output, clear input/output, halt input/output, halt device, test channel and store channel identification.

5. (c)

Maskable interrupt temporally ignored by counter.

6. (c)

Memory size = 4 GB = 2^{32} B

Word size = 2 B

So, unique address = $\frac{2^{32}}{2^1} = 2^{31}$

Hence, atleast 31 bits are required.

7. (a)

Each instruction is stored in one word of memory. Memory is word addressable and 1 word = 24 bits ⇒ 3 bytes.

Total number bits = 24

The instruction set consists of 150 different operations. To generate 150 different operations we need minimum 8 bits are required.

OP code	Address
8	16

So, option (a) is correct.

8. (a)

For direct, EA = address field value in IR (instruction register) = 400

For immediate, actually no meaning of effective address. So, EA here will be just the address of the operand field which is otherwise address field = 301.

For relative addressing, we have EA = PC value (current) + Address field value

EA = 302 + 400 = 702

For register indirect, the EA is the content of the register, the register name being present in the address field of instruction.

So, EA = content of R1 = 200

For indexed mode = Base address + index register content

= 400 + 200 = 600

So, option (a) is correct.

10. (c)

In relative addressing mode content of the program counter is added to the address part of the instruction to get the effective address.

So, option (c) is correct.

11. (b)

- Stack over flow is a internal interrupt.
- Supervisor call is a software interrupt.
- Invalid opcode is a internal interrupt.
- Timer is a external interrupt.

12. (a)

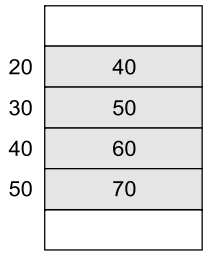
The Jump instruction is at address 3010 H and instruction is 2 bytes. Therefore, PC points to 3012 H on execution of this instruction.

Now Branch Target PC = PC + (–7)

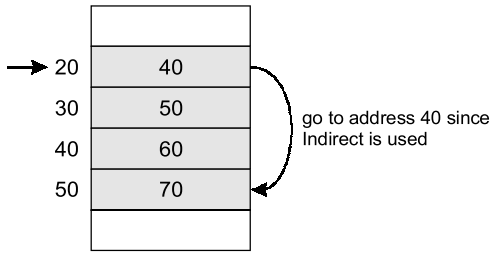
= 3012 H – 7 H = 300 BH

14. (c)

The given information can be understood as



Now load indirect 20 will load 60 into as follows



Hence (c) is correct option.

16. (d)

In immediate addressing mode, the operand is specified in the instruction itself.

For example: MOV R1, 12H is the immediate AM with 12 is operand.

17. (d)

$$\begin{array}{r} 00000010 \\ 00000011 \\ \hline 00000101 \end{array}$$

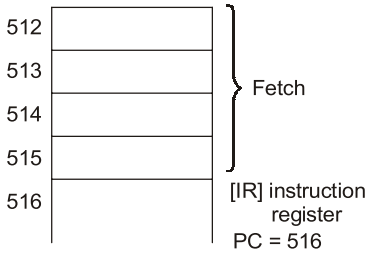
Overflow = 0, sign = 0, half carry = 0

Half carry indicate addition of pack at decimal numbers. When carry takes out of the lower digit order, this flag is set.

Auxiliary carry is also known as half carry.

18. (369)

4 byte instruction storage



Effective address = PC + Relative value

Relative value = EA – PC

= 885 – 516 = (369)10

So, answer is 369.

OPERATING SYSTEM

OBJECTIVE PRACTICE SETS

Page No. 163 - 283

1 CHAPTER
Basic Concepts of Operating System

Multiple Choice Questions & NAT Questions

Q.1 Consider the following code:

```
int n = 5;
while (n > 0)
{
    fork( );
    n--;
}
```

The total number of child processes created is equal to _____.

Q.2 Consider the following program:

```
main( )
{
    for(int i = 0; i < 4; i++)
    {
        fork0;
        fork0;
    }
}
```

The number of child processes created, is equal to _____.

Q.3 The following C program is executed on a Unix/Linux system.

```
# include <unistd.h>
int main( ) {
    int i;
    for (i = 1; i <= 50; i++)
        if (i % 2 == 0 || i % 3 == 0) fork( );
    return 0;
}
```

Then the number of child processes created is equal to _____.

Q.4 Consider the following code:

```
#include <unistd.h>
int main( )
{
    fork( );
    for (i = 1; i <= 5; i++)
    {
        fork( );
        printf("*");
    }
    return 0;
}
```

Then the number of times * is printed, is equal to _____.

Q.5 Which of the following need not necessarily be saved on a context switch between the processes?

(a) Program counter
(b) Stack pointer
(c) Translation lookaside buffer
(d) General purpose registers

Q.6 Which of the following should be allowed only in Kernel mode?

1. Changing mapping from virtual to physical address.
2. Mask and unmask interrupts.
3. Disabling all interrupts.
4. Reading status of processor.
5. Reading time of day.

(a) 1, 2 and 3
(b) 1, 2, 4 and 5
(c) 2, 3 and 5
(d) All of these

Q.7 An interrupt handler is a

(a) location in memory that keeps track of recently generated interrupts
(b) peripheral device
(c) utility program
(d) special numeric code that indicates the priority of a request

Q.8 Executing more than one program concurrently by one user on one computer is known as
(a) multiprogramming (b) time-sharing
(c) multitasking (d) multiprocessing

Q.9 The simultaneous processing of two or more programs by multiple processors is
(a) multitasking (b) multiprogramming
(c) time-sharing (d) multiprocessing

Q.10 Which of the following does not interrupt a running process?
(a) timer interrupts (b) device
(c) power failure (d) scheduling process

Q.11 System call is used to access
(a) I/O functionality
(b) operating system functionality
(c) application functionality
(d) None of the above

Q.12 Swapping is performed by
(a) long term scheduler
(b) mid term scheduler
(c) short term scheduler
(d) dispatcher

Q.13 Choose the false statement
(a) static linking requires no support of OS
(b) dynamic linking requires no support of OS
(c) dynamic loading requires no support of OS
(d) none of the above

Q.14 Assume that the Kernel mode is non-preemptive. What happens when an I/O interrupt comes while a process 'P_1' is running in the Kernel mode on the CPU?
(a) CPU is given to the process for which the I/O has completed
(b) CPU is given to some other process based on the scheduling policy
(c) P_1 continues to execute on the CPU
(d) None of the above

Q.15 Overlay is
(a) a part of an operating system
(b) a specific memory location
(c) a single contiguous memory that was used in the olden days for running large programs by swapping
(d) overloading the system with many user files

Q.16 When an interrupt occurs, an operating system
(a) ignores the interrupt
(b) always changes the stage of the interrupted process after processing the interrupt
(c) always resumes execution of the interrupted process after processing the interrupt
(d) may change the state of the interrupted process to "blocked" and schedule another process

Q.17 Consider the following statements:
S_1: The OS is designed to maximize the resource utilization.
S_2: The control program manages the system programs.
Which of the above statements is/are true?
(a) S_1 is true S_2 is false
(b) S_2 is true and S_1 is false
(c) Both S_1 and S_2 are true
(d) Both S_1 and S_2 are false

Q.18 Bootstrap loader is always stored in
(a) Cache (b) ROM
(c) RAM (d) Disk

Q.19 Which of the following is true?
(a) Overlays are used to increase the size of physical memory.
(b) Overlays are used to increase the logical address space.
(c) When overlays are used, the size of a process is not limited to the size of physical memory.
(d) Overlays are used whenever the physical address space is smaller than the logical address space.

Q.20 Process is
(a) A program in high level language kept on disk
(b) Contents of main memory
(c) A program in execution
(d) A job in secondary memory

Q.21 The state of a process after it encounters an I/O instruction is?
(a) Ready
(b) Blocked
(c) Idle
(d) Running

Q.22 Which of the following statements is true?

(a) Hard real time OS has less jitter than soft real time OS

(b) Hard real time OS has more jitter than soft real time OS

(c) Hard real time OS has equal jitter as soft real time OS

(d) None of the above

Multiple Select Questions (MSQ)

Q.23 Consider a demand-paging system with the following time-measured utilizations:

CPU utilization	20%
Paging disk	97.7%
Order I/O devices	5%

Which (if any) of the following will not (probably) improve CPU utilization?

(a) Install a faster CPU.

(b) Install a bigger paging disk.

(c) Increase the degree of multiprogramming.

(d) Decrease the degree of multiprogramming.

Q.24 Consider a demand-paging system with the following time-measured utilizations:

CPU utilization	20%
Paging disk	97.7%
Order I/O devices	5%

Which (if any) of the following will (probably) improve CPU utilization?

(a) Install more main memory.

(b) Install a faster hard disk or multiple controllers with multiple hard disks.

(c) Add prepaging to the page fetch algorithms.

(d) Increase the page size.

Q.25 Which one of the following is/are true?

(a) Kernel is the program that constitutes the central core of the operating system.

(b) Kernel is the first part of operating system to load into memory during booting.

(c) Kernel is made of various modules which can not be loaded in running operating system.

(d) Kernel remains in the memory during the entire computer session.

Q.26 Which one of the following error will be handle by the operating system?

(a) Power failure

(b) Lack of paper in printer

(c) Connection failure in the network

(d) Disk failure

Q.27 Which of the following statement(s) is/are correct for unix system calls?

(a) exec is used to invokes another program overlaying memory space with a copy.

(b) brk( ) A process synchronizes with termination of child process.

(c) wait is used to increase or decrease the size of data region.

(d) fork is used to creates a new process.

■■■■

Answers Basic Concepts of Operating System

1. (31)	**2.** (255)	**3.** (65535)	**4.** (12)	**5.** (c)	**6.** (a)	**7.** **(c)**	**8.** (c)	**9.** (d)
10. (b)	**11.** (b)	**12.** (b)	**13.** (b)	**14.** (c)	**15.** (c)	**16.** **(d)**	**17.** (a)	**18.** (b)
19. (c)	**20.** **(a)**	**21.** (b)	**22.** (a)	**23.** (a, b, c)	**24.** (a, b, c)	**25.** (a, b, d)	**26.** (a, b, c)	
27. (a, d)								

Explanations Basic Concepts of Operating System

1. (31)

There will be totally 5 fork calls after unrolling the loop, and 5 fork calls lead to $2^5-1 = 31$ child processes. Hence 31 will be the answer.

2. (255)

Unrolling the loop, we have totally 2*4 = 8 fork calls. So with 8 fork calls, we can have $2^8 - 1$, that is, 255 child processes. Hence answer is 255.

3. (65535)

If k is the total number of fork calls, then number of child processes created = $2^k - 1$

Total number of fork calls

= Number of integers between 1 and 50 which are divisible by either 5 or 7

= n(divisible by 5) + n(div by 7) – n(div by 35)

= 10 + 7 – 1 = 16

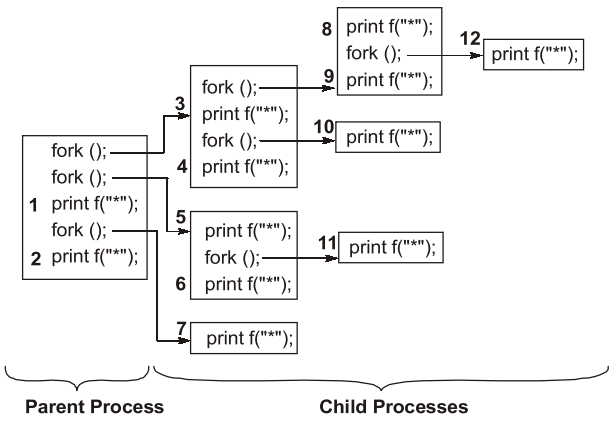
So, number of child processes = $2^{16} - 1 = 65535$.

4. (12)

The code can be reduced to:

```
fork( )
fork( );
printf("*");
fork( );
printf("*");
```

Let's start the trace



Number of times * printed = 12
Therefore (12) is the answer.

5. (c)

PCB doesn't need to save TLB entries during a context switch, as once a CS occurs, the TLB entries may become invalid as the virtual to physical mappings may be irrelevant to the newly scheduled process, so the TLB is generally flushed in this case. Hence (c) is the answer.

6. (a)

Only critical services must reside in the Kernel. All services mentioned except reading status of processors and reading time of the day are critical. Hence option (a) is correct.

14. (c)

When the Kernel is non-preemptive and any process is running in a Kernel mode, then process continues to run until either it completes or it waits for some input/output.

16. (d)

When a interrupt occurs operating system decides the request on the fact that the interrupt has higher priority or less priority. If less, the interrupted process is resumed and only after the execution of process, the interrupt is handled. However if interrupt has higher priority the process is blocked and interrupt is entertained. Hence an operating system may or may not change the state of the interrupted process to "blocked" and schedule another process.

19. (c)

By using the overlays we can execute much greater processes simultaneously which cannot be execute and reside in the memory at the same time. In this the process to be executed process brought to memory only when it is needed at the time of execution.

20. (a)

The program under execution is called process.

21. (b)

The process state diagram is: